EA 7123-I2C

I²C-BUS LCD MIT 3x12 ZEICHEN, SUPERFLACH

Abmessungen:
46x33x2,65mm

TECHNISCHE DATEN

* 3x12 ZEICHEN I²C BUS INTERFACE: 100kHz
* CHIP-ON-GLAS TECHNIK: NUR 2,65mm FLACH
* 5x7 MATRIX, 6°° BLICKRICHTUNG
* DURCH GEDREHTEN ZEICHENSATZ AUCH FÜR 12°° BLICKRICHTUNG
* VERSORUNG +2,5V/-4,5V BIS +6V/-1V @ 500µA
* PCF 2116 ON BOARD
* TRANSFLEKTIV: KANN VON HINTEN BELEUCHTET WERDEN (LED/EL-FOLIE)
* ZEICHENHÖHE 4,7mm
* SICHTFENSTER 32 x 17mm
* AUSSENABMESSUNGEN 46 x 33 mm
* BETRIEBSTEMPERATUR -20... +70°C
* LAGERTEMPERATUR -25... +80°C

BESTELLBEZEICHNUNG

3x12st. DOTMATRIX LCD MIT I²C-BUS EINGANG	**EA 7123-I2C**
LED- BELEUCHTUNGSKÖRPER FÜR 5V / 30mA	**EA LED500-36**

ELECTRONIC ASSEMBLY GMBH
LOCHHAMER SCHLAG 17 · D-82166 GRÄFELFING
TEL 089/8541991 · FAX 089/8541721 · http://www.lcd-module.de

Programming of mux 1 : 32 displays with PCF2114X

To drive a 2-line by 24 characters mux 1 : 32 display, use instruction Function Set M, N to 0, 1. Note that the right half of the display needs mirrored column connection compared to a display driven by a PCF2116X.

To drive a 4-line by 12 characters mux 1 : 32 display the PCF2116 operating instructions apply. There is no functional difference between the two chips in this mode. For such an application set M, N to 1,1 with the Function Set instruction.

Reset function

The PCF2116 automatically initializes (resets) when power is turned on. After reset the chip has the following state.

Table 2 State after reset.

STEP	DESCRIPTION		
1	Display clear.		
2	Function set.	DL = 1	8-bit interface
		M, N = 0	1-line display
		G = 0	voltage generator; $V_{LCD} = V_0$
3	Display on/off control.	D = 0	display off
		C = 0	cursor off
		B = 0	blink off
4	Entry mode set.	I/D = 1	+1 (increment)
		S = 0	no shift
5	Default address pointer to DDRAM. The busy flag (BF) indicates the busy state (BF = logic 1) until initialization ends. The busy state lasts 2 ms. The chip may also be initialized by software. See Figs 28 and 29.		
6	I^2C-bus interface reset.		

INSTRUCTIONS

Only two PCF2116 registers, the instruction register (IR) and the data register (DR) can be directly controlled by the MPU. Before internal operation, control information is stored temporarily in these registers to allow interface to various types of MPUs which operate at different speeds or to allow interface to peripheral control ICs. The PCF2116 operation is controlled by the instructions shown in Table 3 together with their execution time. Details are explained in subsequent sections.

Instructions are of 4 categories, those that:

1. Designate PCF2116 functions such as display format, data length, etc.
2. Set internal RAM addresses.
3. Perform data transfer with internal RAM.
4. Others.

In normal use, category 3 instructions are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of internal RAM addresses after each data write lessens the MPU program load. The display shift in particular can be performed concurrently with display data write, enabling the designer to develop systems in minimum time with maximum programming efficiency.

During internal operation, no instruction other than the busy flag/address read instruction will be executed.

Because the busy flag is set to logic 1 while an instruction is being executed, check to make sure it is on logic 0 before sending the next instruction or wait for the maximum instruction execution time, as given in Table 3. An instruction sent while the busy flag is HIGH will not be executed.

Table 3 Instructions (note 1).

INSTRUCTION	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	REQUIRED CLOCK CYCLES[2]
NOP	0	0	0	0	0	0	0	0	0	0	no operation	0
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DDRAM address 0 in address counter.	165
Return Home	0	0	0	0	0	0	0	0	1	0	Sets DDRAM address 0 in address counter. Also returns shifted display to original position. DDRAM contents remain unchanged.	3
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operations are performed during data write and read.	3
Display control	0	0	0	0	0	0	1	D	C	B	Sets entire display on/off (D), cursor on/off (C) and blink of cursor position character (B).	3
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	0	0	Moves cursor and shifts display without changing DDRAM contents.	3
Function set	0	0	0	0	1	DL	N	M	G	0	Sets interface data length (DL), number of display lines (N, M) and voltage generator control (G).	3
Set CGRAM address	0	0	0	1	A_{CG}						Sets CGRAM address	3
Set DDRAM address	0	0	1	A_{DD}							Sets DDRAM address	3
Read Busy Flag and Address Counter	0	1	BF	A_C							Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0
Read data	1	1	read data								Reads data from CGRAM or DDRAM.	3
Write data	1	0	write data								Writes data to CGRAM or DDRAM.	3

Notes

1. In the I²C-bus mode the DL bit is don't care. 8-bit mode is assumed.
   In the I²C-bus mode a control byte is required when RS or R/$\overline{W}$ is changed; control byte: Co, RS, R/$\overline{W}$, 0, 0, 0, 0, 0; command byte: DB7 to DB0.
2. Example: f_{osc} = 150 kHz, $T_{cy} = \frac{1}{f_{osc}}$ = 6.67 µs; 3 cycles = 20 µs, 165 cycles = 1.1 ms.

Table 4 Command bit identities.

BIT	0	1
I/D	decrement	increment
S	display freeze	display shift
D	display off	display on
C	cursor off	cursor on
B	character at cursor position does not blink	character at cursor position blinks
S/C	cursor move	display shift
R/L	left shift	right shift
DL	4 bits	8 bits
G	voltage generator: $V_{LCD} = V_0$	voltage generator; $V_{LCD} = V_0 - 0.8V_{DD}$
N, (M = 0) PCF2116 PCF2114	 1 line × 24 characters; mux 1 : 16 2 line × 12 characters; mux 1 : 16	 2 lines × 24 characters; mux 1 : 32 2 lines × 24 characters; mux 1 : 32
N, (M = 1)	reserved	4 lines × 12 characters; mux 1 : 32
BF	end of internal operation	internal operation in progress
Co	last control byte, only data bytes to follow	next two bytes are a data byte and another control byte

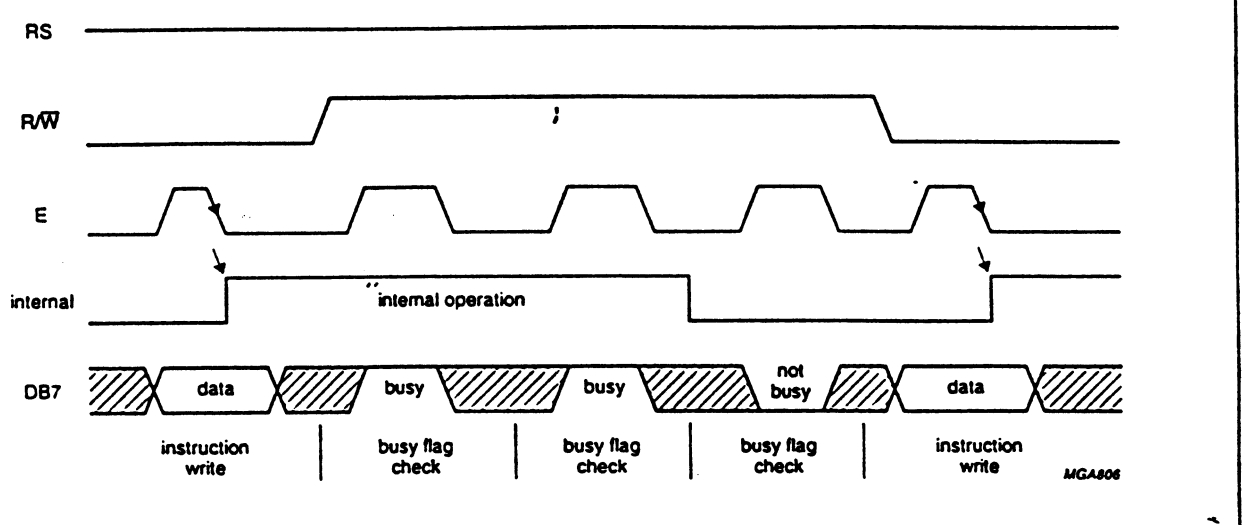


Fig.20 Example of busy flag check timing sequence.

Clear display

Clear Display writes space code 20 (hexadecimal) into all DDRAM addresses (The character pattern for character code 20 must be blank pattern). Sets the DDRAM address counter to logic 0. Returns display to its original position if it was shifted. Thus, the display disappears and the cursor or blink position goes to the left edge of the display (the first line if 2 or 4 lines are displayed). Sets entry mode I/D = logic 1 (increment mode). S of entry mode does not change.

The instruction Clear Display requires extra execution time. This may be allowed for by checking the busy-flag (BF) or by waiting until 2 ms has elapsed. The latter must be applied where no read-back options are foreseen, as in some chip-on-glass (COG) applications.

Return Home

Return Home sets the DDRAM address counter to logic 0. Returns display to its original position if it was shifted. DDRAM contents do not change. The cursor or blink position goes to the left of the display (the first line if 2 or 4 lines are displayed). I/D and S of entry mode do not change.

Entry mode set

ID

When I/D = logic 1 (0) the DDRAM or CGRAM address increments (decrements) by 1 when data is written into or read from the DDRAM or CGRAM. The cursor or blink position moves to the right when incremented and to the left when decremented. The cursor and blink are inhibited when the CGRAM is accessed.

S

When S = logic 1, the entire display shifts either to the right (I/D = logic 0) or to the left (I/D = logic 1) during a DDRAM write. Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DDRAM, or when writing into or reading out of the CGRAM. When S = logic 0 the display does not shift.

Display on/off control

D

The display is on when D = logic 1 and off when D = logic 0. Display data in the DDRAM are not affected and can be displayed immediately by setting D to logic 1.

C

The cursor is displayed when C = logic 1 and inhibited when C = logic 0. Even if the cursor disappears, the display functions I/D, etc. remain in operation during display data write. The cursor is displayed using 5 dots in the 8th line (see Fig.12).

B

The character indicated by the cursor blinks when B = logic 1. The blink is displayed by switching between display characters and all dots on with a period of 1 second when f_{osc} = 150 kHz (Fig.12). At other clock frequencies the blink period is equal to 150 kHz/f_{osc}. The cursor and the blink can be set to display simultaneously.

Cursor or display shift

Cursor or Display Shift moves the cursor position or the display to the right or left without writing or reading display data. This function is used to correct a character or move the cursor through the display. In 2 or 4-line displays, the cursor moves to the next line when it passes the last position (40 or 20 decimal) of the line. When the displayed data is shifted repeatedly all lines shift at the same time; displayed characters do not shift into the next line. The address counter (AC) content does not change if the only action performed is shift display, but increments or decrements with the cursor shift.

Function set

DL (PARALLEL MODE ONLY)

Sets interface data width. Data is sent or received in bytes (DB7 to DB0) when DL = logic 1 or in two nibbles (DB7 to DB4) when DL = logic 0. When 4-bit width is selected, data is transmitted in two cycles using the parallel bus(1).

Function set from I²C-interface: DL bit can not bet set to 0 from the I²C-interface. If bit DL has been set to 0 via the parallel bus, programming via the I²C-interface is complicated.

N, M

Sets number of display lines.

G

Controls the V_{LCD} voltage generator characteristic.

Set CGRAM address

Set CGRAM Address sets bit 0 to 5 of the CGRAM address ACG into the address counter (binary $A_5A_4A_3A_2A_1A_0$). Data can then be written to or read from the CGRAM.

Only bits 0 to 5 of the CGRAM address are set by the set CGRAM address command. Bit 6 can be set using the set DDRAM address command or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the read BF and address command.

Set DDRAM address

Set DDRAM Address sets the DDRAM address into the address counter (binary $A_6A_5A_4A_3A_2A_1A_0$). Data can then be written to or read from the DDRAM.

Hexadecimal address ranges.

ADDRESS	FUNCTION
00 to 4F	1-line by 24; 2116
00 to 0B and 0C to 4F	2-line by 12; 2114
00 to 27 and 40 to 67	2-line by 24; 2114/2116
00 to 13, 20 to 33, 40 to 53 and 60 to 73	4-line by 12; 2114/2116

Read busy flag and address

Read Busy Flag and Address reads the busy flag (BF). BF = logic 1 indicates that an internal operation is in progress. The next instruction will not be executed if BF = 1. Check the BF status before sending the next instruction.

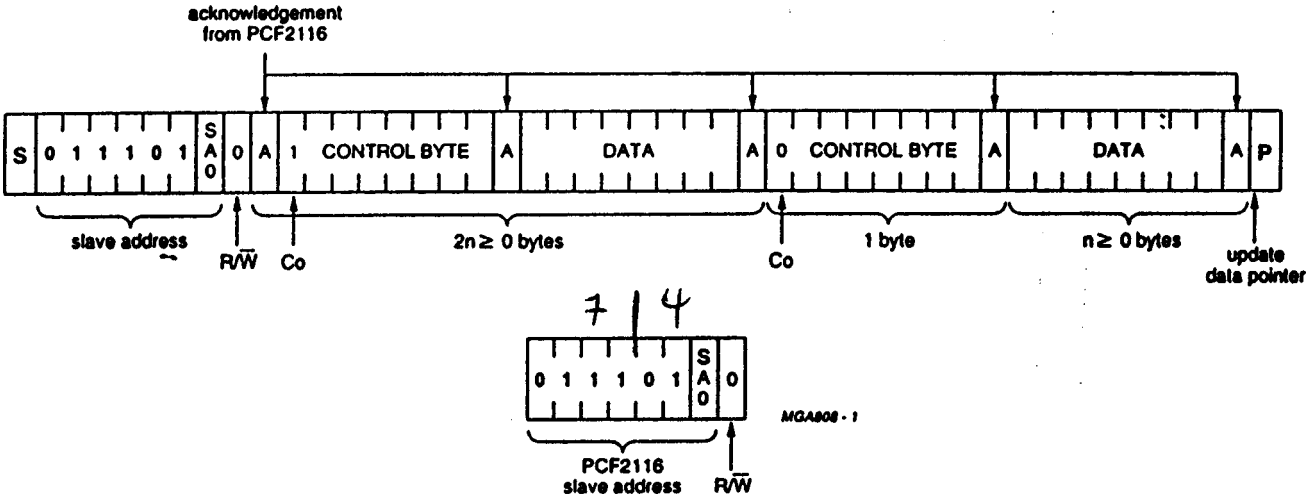
At the same time, the value of the address counter expressed in binary A_6 to A_0 is read out. The address counter is used by both CGRAM and DDRAM, and its value is determined by the previous instruction.

Write data to CGRAM or DDRAM

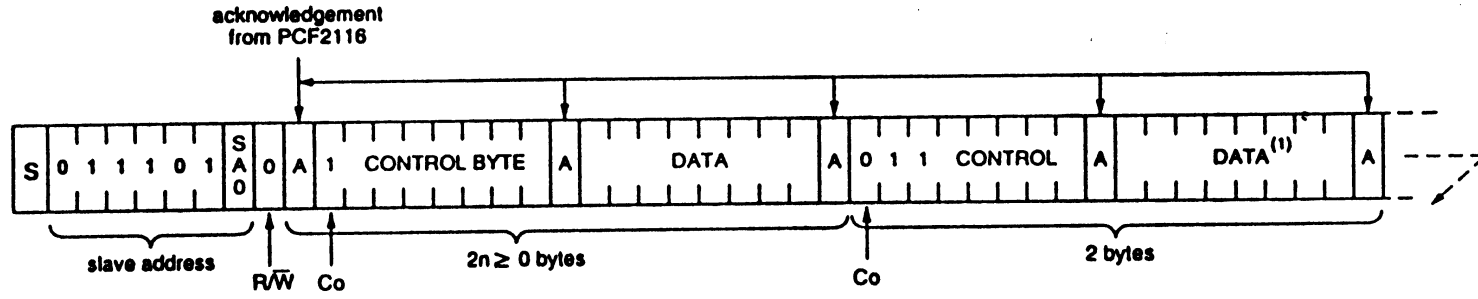
Writes binary 8-bit data D_7 to D_0 to the CGRAM or the DDRAM.

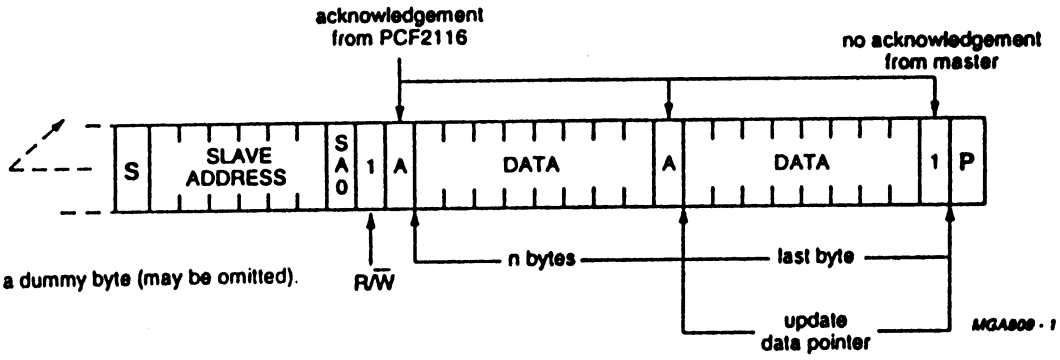
Whether the CGRAM or DDRAM is to be written into is determined by the previous specification of CGRAM or DDRAM address setting. After writing, the address automatically increments or decrements by 1, in accordance with the entry mode. Only bits D0 to D4 of CGRAM data are valid, bits D5 to D7 are 'don't care'.

(1) In a 4-bit application DB3 to DB0 are left open (internal pull-ups). Hence in the first function set instruction after power-on G and H are set to 1. A second function set must then be sent (2 nibbles) to set G and H to their required values.

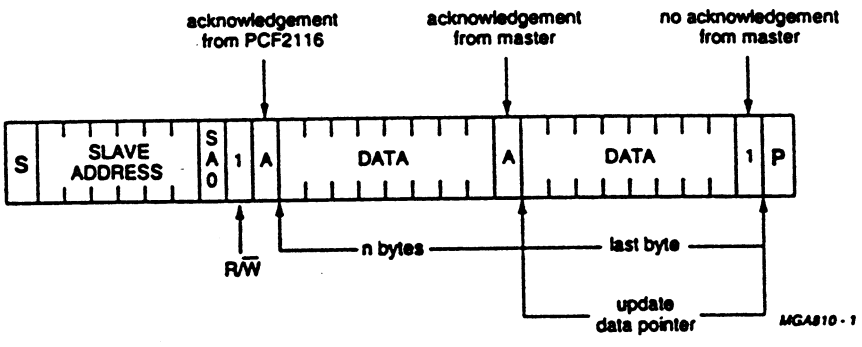


Master transmits to slave receiver; WRITE mode.





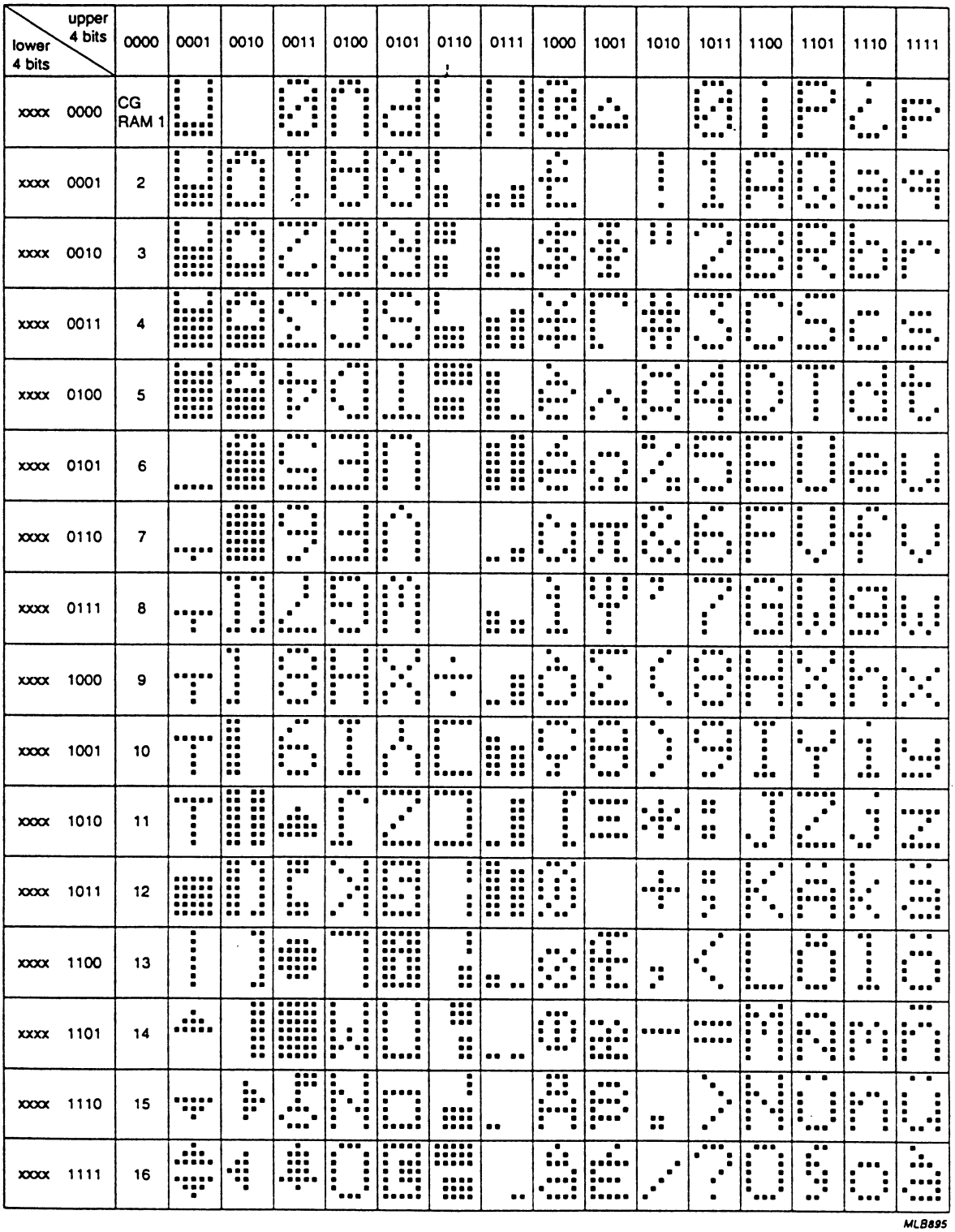
(1) Last data byte is a dummy byte (may be omitted).



Master reads slave immediately after first byte; READ mode (RS previously defined).

ELECTRONIC ASSEMBLY

FONT TABELLE CHARACTERSET -C



Character set 'C' in CGROM; PCF2116C;

Table 8 Example of I²C operation; 1-line display (using internal reset, assuming SA0 = V_{SS}; note 1).

STEP	I²C BYTE	DISPLAY	OPERATION
1	I²C start		Initialized. No display appears.
2	Slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1		During the acknowledge cycle SDA will be pulled-down by the PCF2116.
3	Send a control byte for function set Co RS R/$\overline{W}$ Ack 0 0 0 X X X X X 1		Control byte sets RS and R/$\overline{W}$ for following data bytes.
4	Function set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 1 X 1 1 0 0 1		Selects 4-line display and $V_{LCD} = V_0$; SCL pulse during acknowledge cycle starts execution of instruction.
5	Display on/off control DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 1 1 1 0 1	_	Turns on display and cursor. Entire display shows character hex 20 (blank in ASCII-like character sets).
6	Entry mode set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 1 1 0 1	_	Sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DDRAM or CGRAM. Display is not shifted.
7	I²C start	_	For writing data to DDRAM, RS must be set to 1. Therefore a control byte is needed.
8	Slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1	_	
9	Send a control byte for write data Co RS R/$\overline{W}$ Ack 0 1 0 X X X X X 1	_	
10	Write data to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 0 0 1	 P_	Writes 'P'. The DDRAM has been selected at power-up. The cursor is incremented by 1 and shifted to the right.

STEP	I²C BYTE	DISPLAY	OPERATION
11	Write data to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 1	PH_	Writes 'H'.
12 to 15			
16	Write data to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 1 1 1	PHILIPS_	Writes 'S'.
17	(optional I²C stop) I²C start + slave address for write (as step 8)	PHILIPS_	
18	Control byte Co RS R/$\overline{W}$ Ack 1 0 0 X X X X X 1	PHILIPS_	
19	Return Home DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 0 1 0 1	PHILIPS	Sets DDRAM address 0 in address counter. (also returns shifted display to original position. DDRAM contents unchanged). This instruction does not update the Data Register (DR).
20	Control byte for read Co RS R/$\overline{W}$ Ack 0 1 1 X X X X X 1	PHILIPS	DDRAM content will be read from following instructions. The R/$\overline{W}$ has to be set to 1 while still in I²C-write mode.
21	I²C start	PHILIPS	
22	Slave address for read SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 1 1	PHILIPS	During the acknowledge cycle the content of the DR is loaded into the internal I²C interface to be shifted out. In the previous instruction neither a Set Address nor a Read Data has been performed. Therefore the content of the DR was unknown.
23	Read data: 8 x SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack X X X X X X X X 0	PHILIPS	8 x SCL; content loaded into interface during previous acknowledge cycle is shifted out over SDA. MSB is DB7. During master acknowledge content of DDRAM address 01 is loaded into the I²C interface.

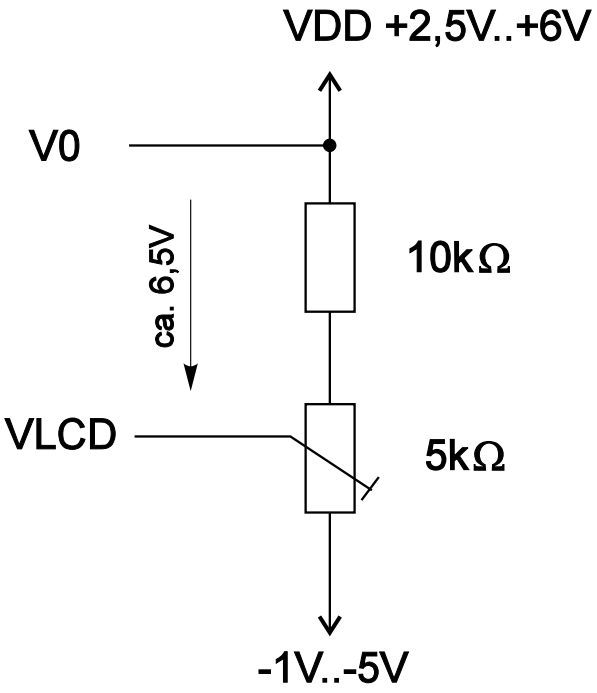
STEP	I²C BYTE	DISPLAY	OPERATION
24	Read data: 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 0	PHILIPS	8 × SCL; code of letter 'H' is read first. During master acknowledge code of 'I' is loaded into the I²C interface.
25	Read data: 8 × SCL + no master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 1 1	PHILIPS	No master acknowledge; After the content of the I²C interface register is shifted out no internal action is performed. No new data is loaded to the interface register, Data Register (DR) is not updated, Address Counter (AC) is not incremented and cursor is not shifted.
26	I²C stop	PHILIPS	

Notes

1. X = don't care.
2. SDA is left at high-impedance by the microcontroller during the READ acknowledge.

EA 7123-I2C muss anders als in diesem Beispiel von Philips auf 4-zeilig initialisiert werden (N=1 und M=1). Eventuell muß auch noch der Negativgenerator akiviert werden!

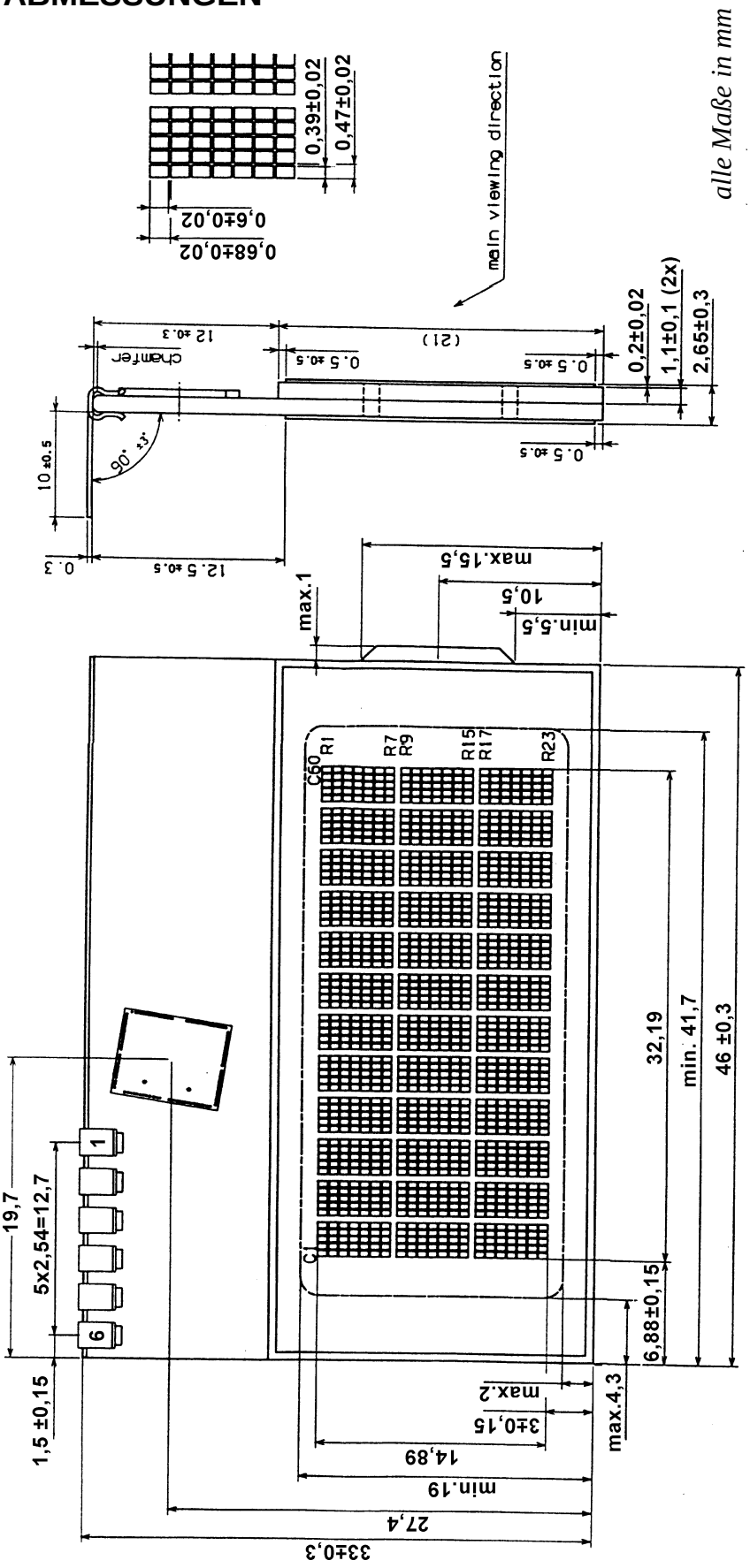
KONTRASTEINSTELLUNG



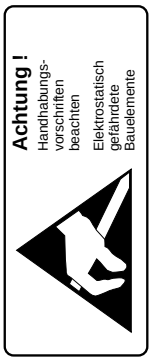
Function set: *Bit G=0 (V_{LCD}=V_0)*
Bit M=1 (3-4 lines)
Bit N=1 (3-4 lines)

EA 7123-I2C

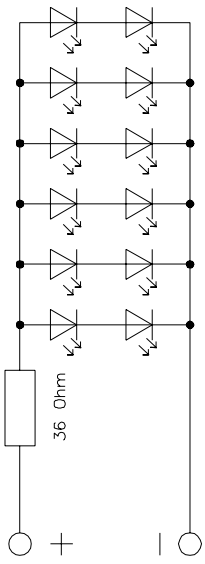
ABMESSUNGEN



Pinout EA 7123-I2C		
Pin	Symbol	Function
1	VSS	Ground
2	VDD	Power Supply
3	VLCD	Contrast adjust
4	V0	Power for contrast
5	SDA	Serial Data Line
6	SCL	Serial Clock Line



Note:
EA 7123-I2C must not be soldered direct onto pcb. Keep a distance of 5mm in minimum between pcb and lcd to avoid damage by soldering heat.



Innenschaltung des optionalen Beleuchtungskörpers EA LED500-36.
Bauhöhe 5mm.

LOCHHAMER SCHLAG 17 · D - 82166 GRÄFELFING
TEL 089/8541991 · FAX 089/8541721 · http://www.lcd-module.de

ELECTRONIC ASSEMBLY GMBH